**SIMULATION AND ANALYSIS OF 6T SRAM CELL USING POWER REDUCTION TECHNIQUES**

ABSTRACT

The demand for static random-access memory (SRAM) is increasing with large use of SRAM in System On-Chip and high-performance VLSI circuits. The high-density VLSI circuits and the exponential dependency of the leakage current on the oxide thickness is becoming a major challenge in deep-sub-micron CMOS technology. As the density of SRAM increases, the leakage power has become a significant component in chip design. This paper represents the simulation of 6T SRAM cells using low power reduction techniques and their comparative analysis on different parameters such as Power Supply Voltage, Delay, Operating Temperature and area efficiency etc. In comparison to the conventional 6T SRAM bit-cell, the total leakage power is reduced. All the simulations have been carried out on BSIM 3V3 90nm and 45nm at Tanner EDA tool.

**TOOLS REQUIRED:**

* DSCH
* MICROWIND